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DESIGN AND IMPLEMENTATION OF ELECTROCARDIOGRAM (ECG) SIGNAL GENERATOR BASED ON FPGA

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ABSTRACT

This paper offers a hardware design to produce a programmable ECG-channels signal generator using only a Field Programmable Gate Array (FPGA) and a small number of passive external components. The FPGA is used to create a new technique using linearised pulse width modulation (PWM) scheme, which would not be possible with other alternatives technologies such as a microcontroller. This system can be used in the testing of multi-inputs ECG system without needing to use a human or extra testing cost. This approach is developed to improve accuracy of the signal waveform without increasing the hardware or complexity, the overall system takes up only 30% of the available FPGA slices. The system described has applicability in other areas where multiple, time skewed and low voltage signals are required. The waveform signal for each channel can be modified easily to match the need of the application. The application of ECG generator has many advantages such as reducing the test time and simplifies the use of ECG signals without need for invasive and non-invasive methods.

KEYWORDS: Electrocardiogram (ECG), FPGA, PWM, Signal Generator, Verilog *HDL*.

INTRODUCTION

The heartbeat of any person can be used to examine cardiovascular (CV) health, the common technique used to monitoring heartbeat is Electrocardiogram (ECG). An ECG monitoring system consists from an electrodes sensor and acquisition device, which is used for sensing the heart activity. A PWM has been used in the last years in applications for biomedical for signal processing such as ENG and EMG signal generator [1-5]. Several techniques have already been proposed in previous works for generation ECG signal based on hardware design [2], such as FPGA [6] and micro controller [2], however these systems required large size of hardware and high cost.

The use of FPGAs for signals generator tasks is well established [7]. This is mainly due to their configurability and programmability. In addition, the FPGA is easily configured to create a one bit PWM outputs and implement precision improvements on these outputs [8].

Previous studies have presented a scrambler as part of a data weight averaging algorithm (DWA) for a delta sigma DAC [3],[9]. The proposal design offers an artificial ECG signal generator consist of a twelve channels, while the system is implemented using only one FPGA board and a small number of passive external components. Moreover, this concept is modified to create a novel, linearised Pulse Width Modulation (PWM) scheme, which would not be possible with other alternatives technologies such as a microcontroller. This signal generator has been used to simulate heartbeat of any person without needing to resort to the use of a human. Techniques are developed to improve precision of the signal waveform without increasing cost or hardware complexity. In addition, the design is implemented in a platform independent hardware description language (HDL) on an XC3S250E FPGA board. A USB interface is used to provide the flexibility to control the artificial heartbeat rate.

SYSTEM COMPONENTS

The block diagram of the system, which is used to generate twelve channels of simulated ECG signal is shown in Fig.1. This system consists of a FPGA based digital controller with a usb interface to the laptop as shown in Fig.2. The controller drives a multi-channel low pass filter with a PWM sequence that follows the desired ECG waveform. The controller makes use of an off-the-shelf Digilent Basys 2 board, which includes a usb interface. Uncommitted digital outputs from the Basys 2 are used as the PWM channel outputs. Each PWM output is connected to an analogue low pass filter.

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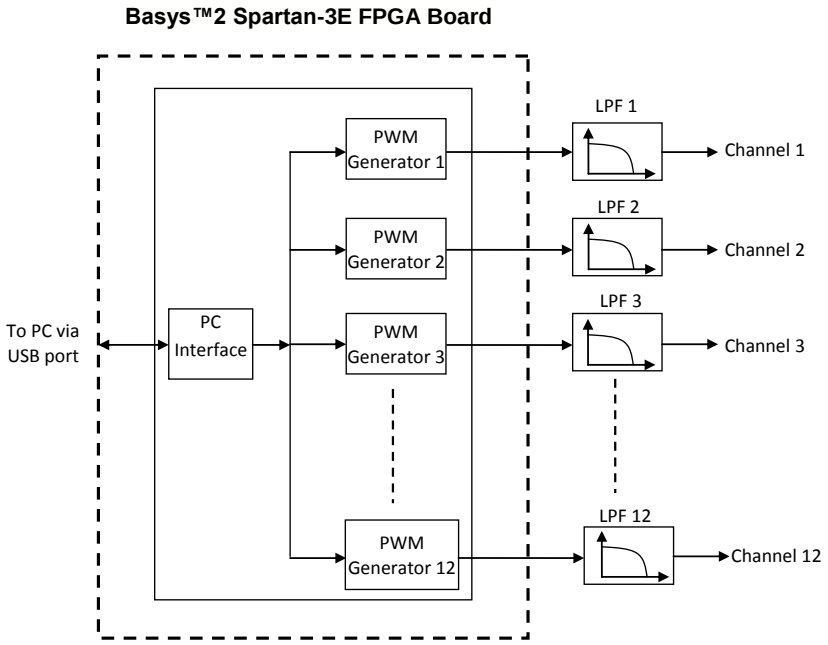

Figure 1. Block diagram of ECG simulation system

Figure 2: The design is implemented on FPGA board (XC3S250E) with a usb interface to provide the flexibility to adjust the ECG signal.

FPGA Unit

The digital hardware portion of the controller is written in Verilog and synthesized using the Xilinx ISE workflow. The design has been verified using a combination of bench testing and simulation using ModelSim, Matlab and oscilloscope.

The on-board 50 MHz clock is used as the timing reference for the PWM generator. For the required 10 bit data precision, the PWM sample rate is kept at just under 50kHz (48.8kHz to be exact), which is adequate for the generation of ECG signals. The overall system takes less than 30% of the available FPGA slices, thereby suggesting that further savings could be achieved if the design was implemented on a custom circuit board.

Low Pass Filter Unit

Fig. 3 shows the low pass filter, which consists of a simple an RC filter to further reduce the magnitude of high frequency components. Each PWM signal is fed through one of these networks to produce one channel of the ECG waveform.

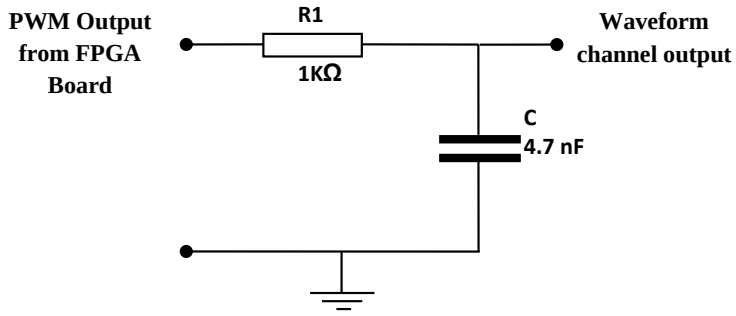

Figure 3. The low pass filter.

HDL Design

A novel linearised technique is used for the signal generator design based on PWM method in this study, which is already proposed in our previous study [3]. The PWM generator and Linearization method based on scrambler technique[3], [9]. Verilog hardware described language design (HDL) has been used for synthesis and designs the whole system during the implementation on the FPGA board. This provides the flexibility to re-synthesise to a standard cell library for an appropriate silicon process such as, the Austria Microsystems 0.35µm process [3].

In addition, the results with experimental measurement made on the test bench demonstrated here as well as oscilloscope traced. The experimental and simulation results of outputs show significant performances on the signal generator after the linearisation process.

The controller produces a PWM output ,which is filtered to reproduce a standard ECG waveform ,which represented in Fig.4 The characteristics of ECG signal is demonstrated the main signal features, which are the P, Q, R, S, and T waves, the period of each wave and time intervals for each element such as the P-R, S-T and Q-T period.

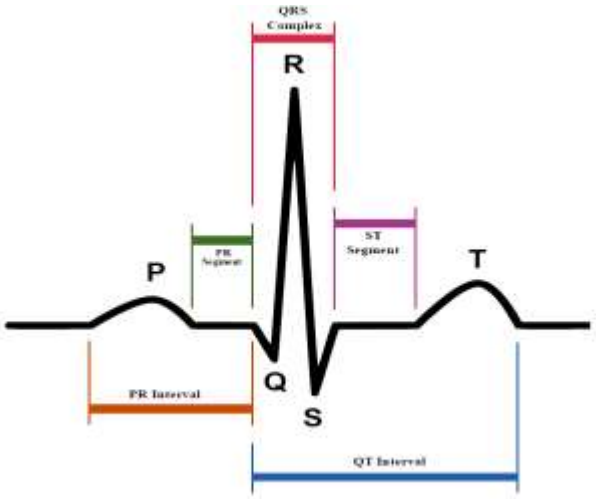

Figure 4. Normal ECG signal of a heart[10].

In addition, the values of P, Q, R, S and T waves are changeable parameters to allow for the user to change the waveform, amplitude and time period. As a result, this offers flexible options for the user to change heartbeats faster or slower without the need to modify the hardware design or the software code. Moreover, the usb controller interface has been presented in this system to allow the user to utilize the PC for controlling the FPGA Board faster. Initially, the sample points of ECG waveform were taken to be 32 samples as an optimum sampling frequency of 48.828k sample/sec. (50MHz/1024) as shown in Fig. 5.

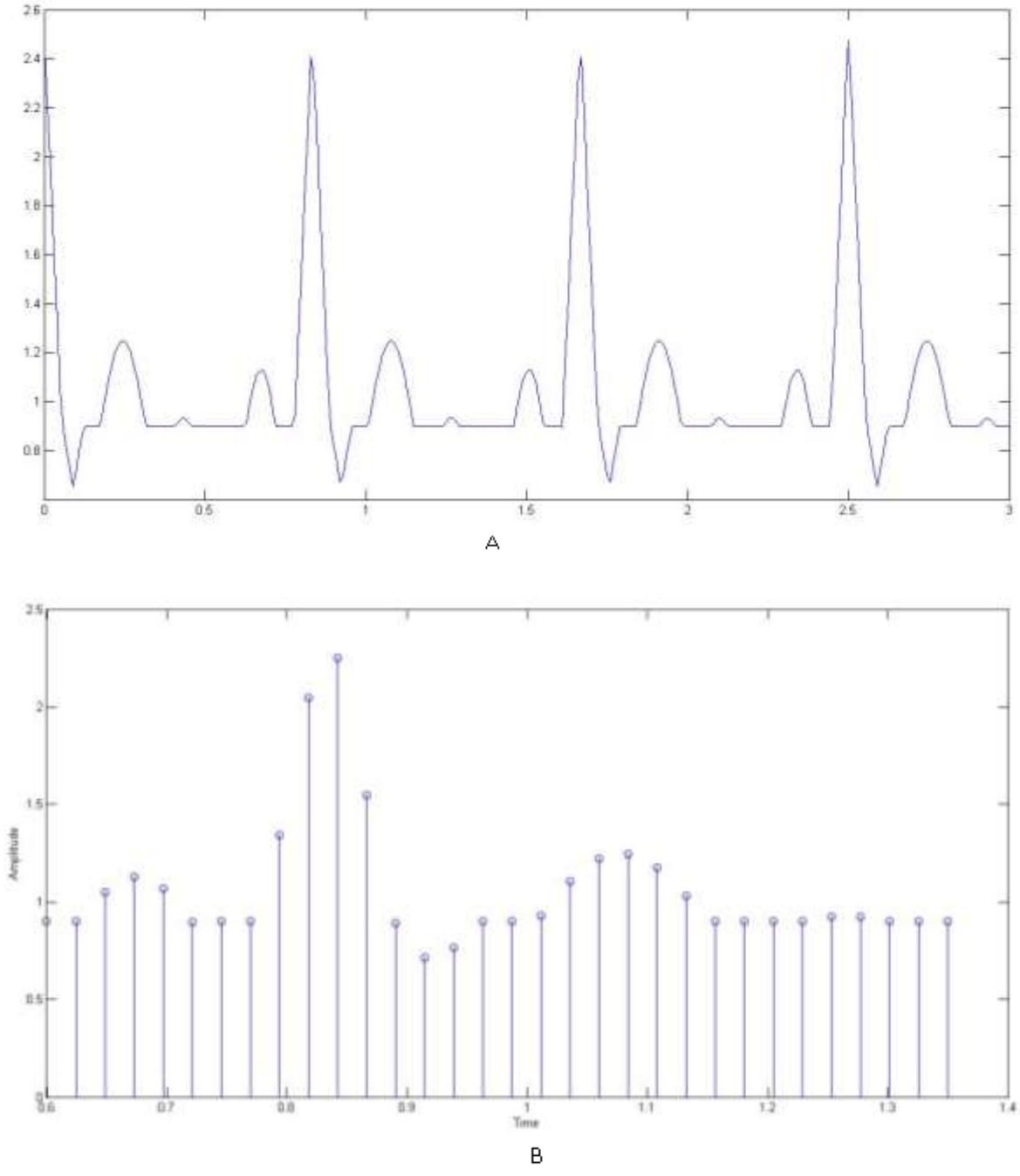

Figure 5: (A) Simulated ECG signal in Matlab, (B) 32 Sample points of the ECG signal

Each sample point of the ECG signal is represented by a 10 bit binary number, scaled to the system output range (3.3V) and then stored in the 32x10 ROM that has been created on the FPGA. The system output for each channel is

PWM digital output from the FPGA, filtered by the simple RC low-pass filter to convert the signal from digital to analogue. The low pass filter is chosen to have a 3dB point at approximately 212 kHz and output impedance about 5 kΩ. This gives a flat response in the frequency range of interest and provides the system under test with biologically plausible source impedance. Fig.6 shows the system used to generate the one bit PWM output.

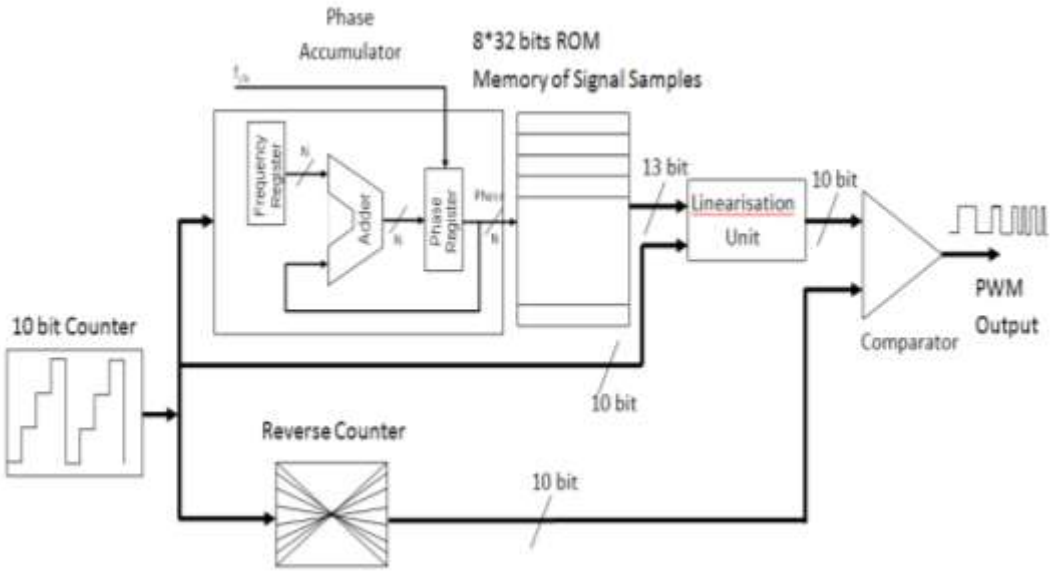

Figure 6: The PWM generation architecture

The PWM generation architecture shown in Fig. 6 consists of six parts:

- A phase accumulator, which provides the sample ROM with index of the current sample.
- A sample ROM, which has 32 samples represented as a 10-bit fixed-point value. The values for this ROM are calculated in Matlab and output as a hexadecimal data list that can be loaded into the ROM using a Verilog HDL readmemh() command.
- A linearisation unit, Which is used for removing the ripple voltage in the ECG waveform and produce a straight line between waveform sample points
- A scrambler ,which takes the input count value and swaps the order of the bits so that the most significant counter bit becomes the least significant and vice-versa .
- An output comparator that compares the sample from linearisation unit output with the scrambled counter output. This produces the final PWM output.

Since the counter goes through the full range of values that can be represented by the 10 bit output, scrambling the counter output by bit reversing it, only changes the order in ,which the output values appear, however it has the advantage of spreading the induced noise to higher frequencies ,which are then filtered by the output low pass filter. This technique is used successfully in pervious researches in different application [3].

Linearization the Generated AP Waveform

Once the PWM output of the FPGA has been passed through the low pass filter to generate the ECG waveform, it can be observed as an analogue signal. Since the sample rate is 48.8kSample/s, the charging curve of the capacitor in the low pass filter is still observable. The CR charging ripple is removed in the ECG waveform and produced a straight line between waveform sample points. The new module makes use of the scrambling process which spreads the 1 and 0 output values through the whole PWM period. This allows the output comparator to be fed with a changing value for the reference input. The reference value is modified such that it provides a constant voltage differential across the filter input resistor which in turn creates a linear change of voltage on the smoothing capacitor. The linearisation uses a fixed point form as shown in the eqn.(1)[3]:

$$PWM\_Value = V_i + (0.264 + 0.927 \times P) \times (V_{i+1} - V_i) \quad (1)$$

Where V_i and V_{i+1} are successive sample values from memory and P is a value in the range 0 to 1.0 indicating the current position within the PWM cycle. In the fixed point implementation, P is simply the non-reversed counter output. The constants were found experimentally for a range of successive sample pairs. PWM Value is the input to comparator as shown in Fig.7.

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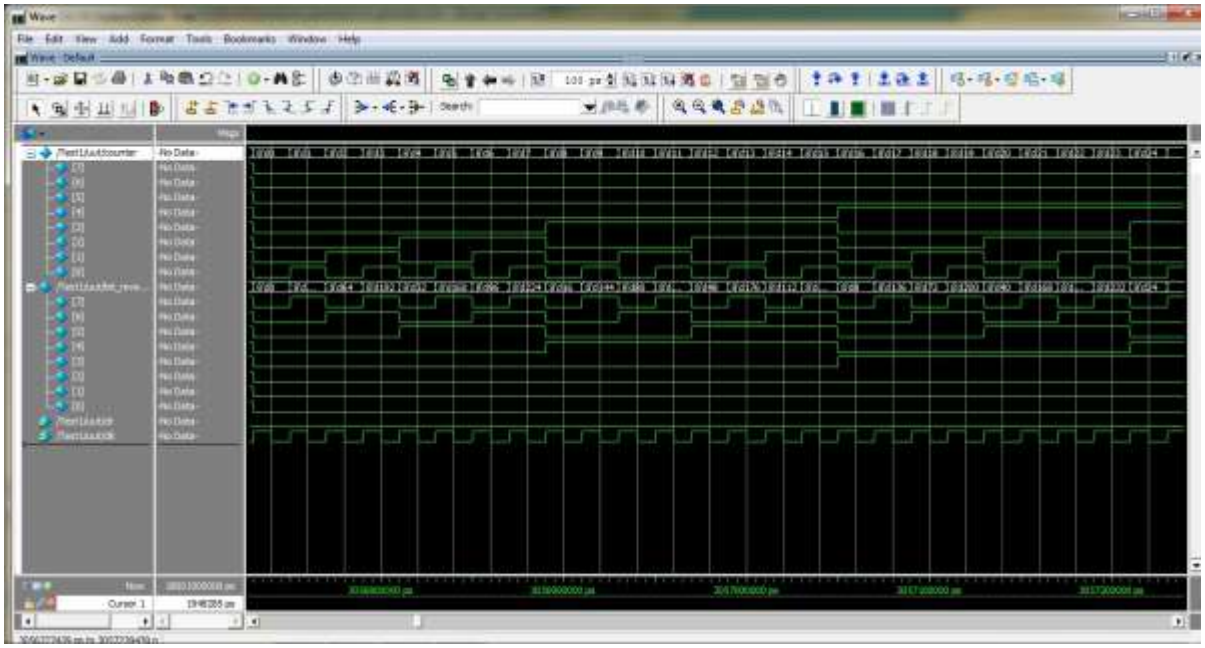

Figure 7: The linearised method with PWM and with scrambler technique

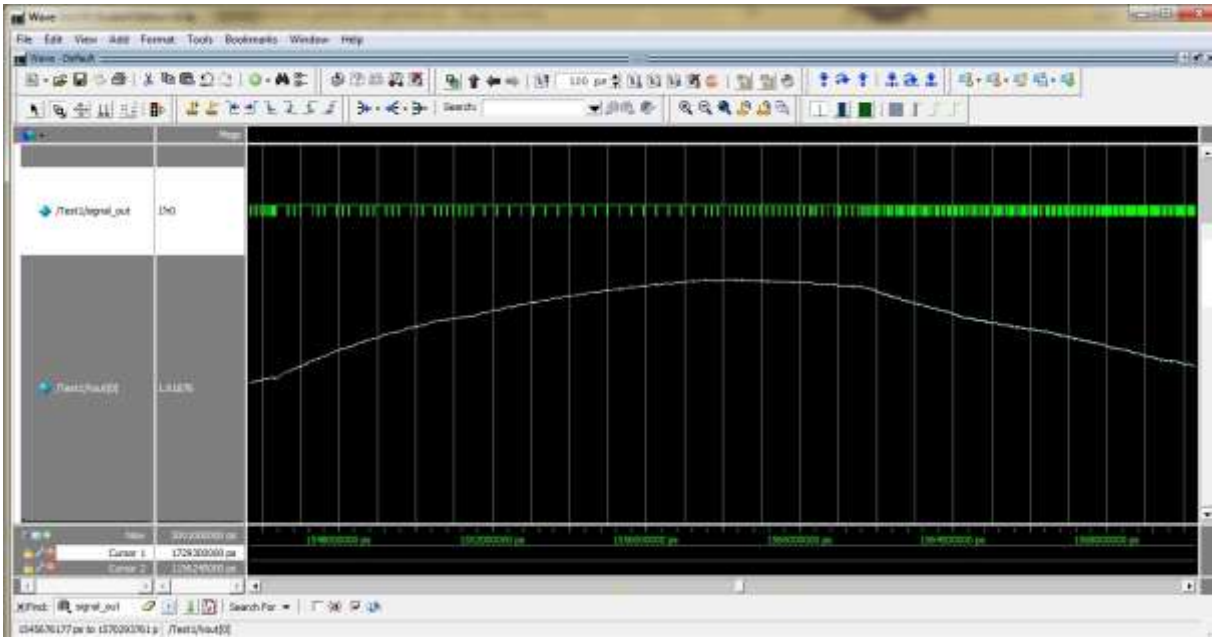

Figure 8: The signal output for the ECG generator with linearised method before and after LPF respectively.

Further simulations and test using Matlab and oscilloscope have been applied to verify and examine the system algorithm behave, which shown in Figs. 9 and 10 respectively. The RC smoothing in this simulation is selected to demonstrate the variation between the scrambled output PWM and normal PWM. The output of each stage is shown clearly in simulation plot as well as the significant improvements on the output of scrambler.

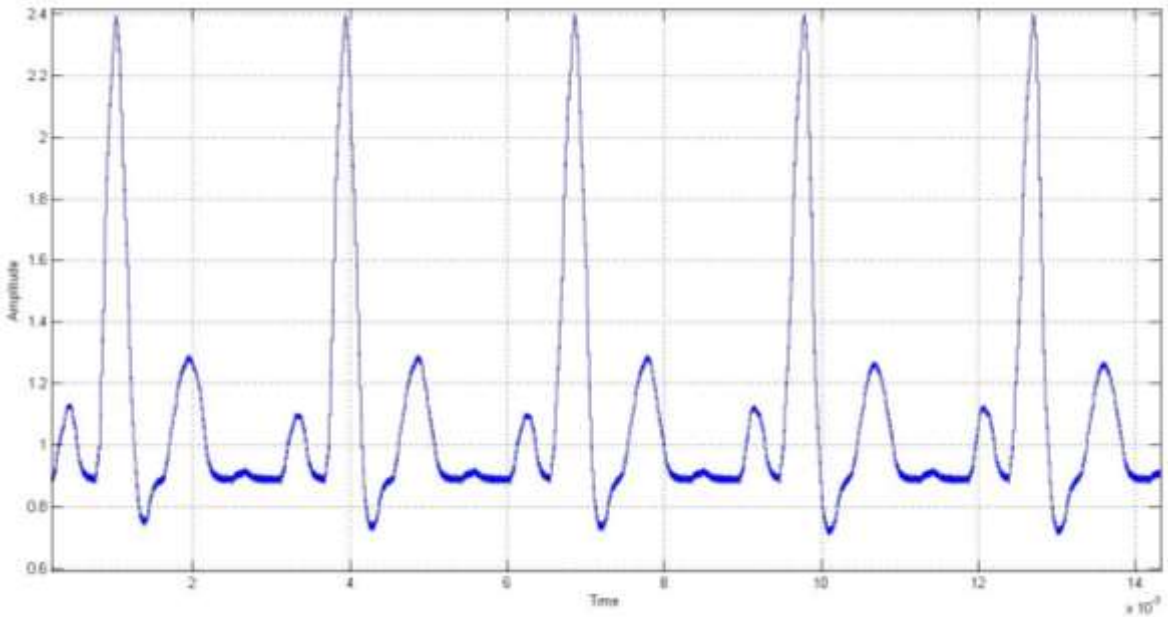

Figure 9: The ECG waveform output data plotted in Matlab.

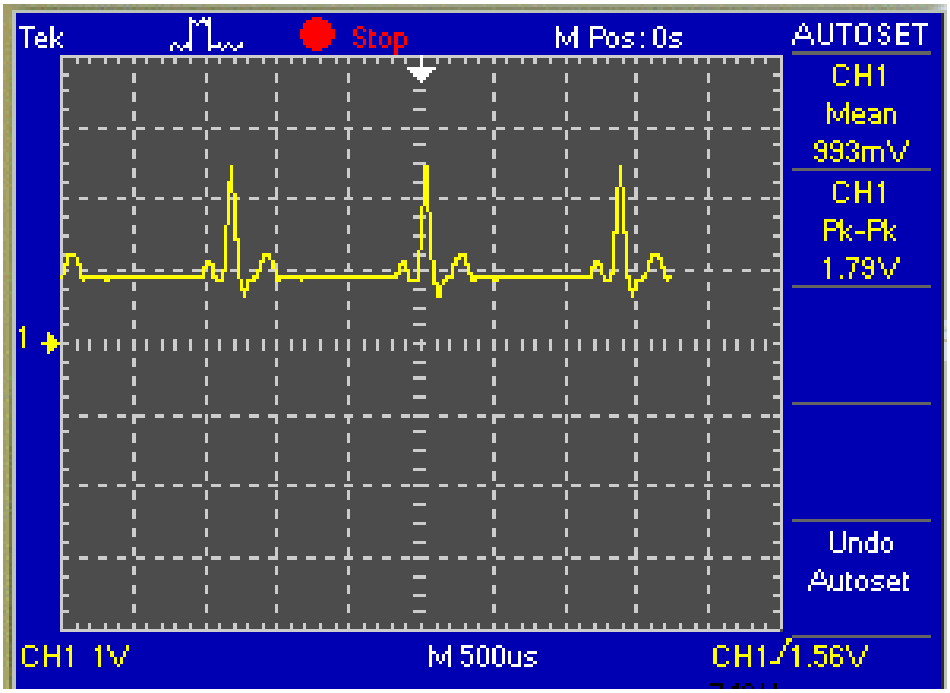

Figure 10: The artificial ECG waveform in oscilloscope trace.

RESULTS AND DISCUSSION

A composite module was created for a test it was tested on both outputs, the linearised and non-linearised PWM signals. The output waveform from the linearize PWM contains almost no ripples as shown in Figs. 9 and 10 ,which shows the Matlab plot and oscilloscope trace taken from the filtered output. Fig. 11 shows the FPGA board, which includes simulation of multi-channel ECG generator with rank of LPF. Moreover, The system this system is capable of generating twelve channels of ECG signal with heart rate from 60-90 bpm with an adjustable waveform, with signal feature PR Interval: 0.12 - 0.20 sec, QRS duration: 0.06 - 0.10 sec, QT interval (QTc $\leq$ 0.40 sec).

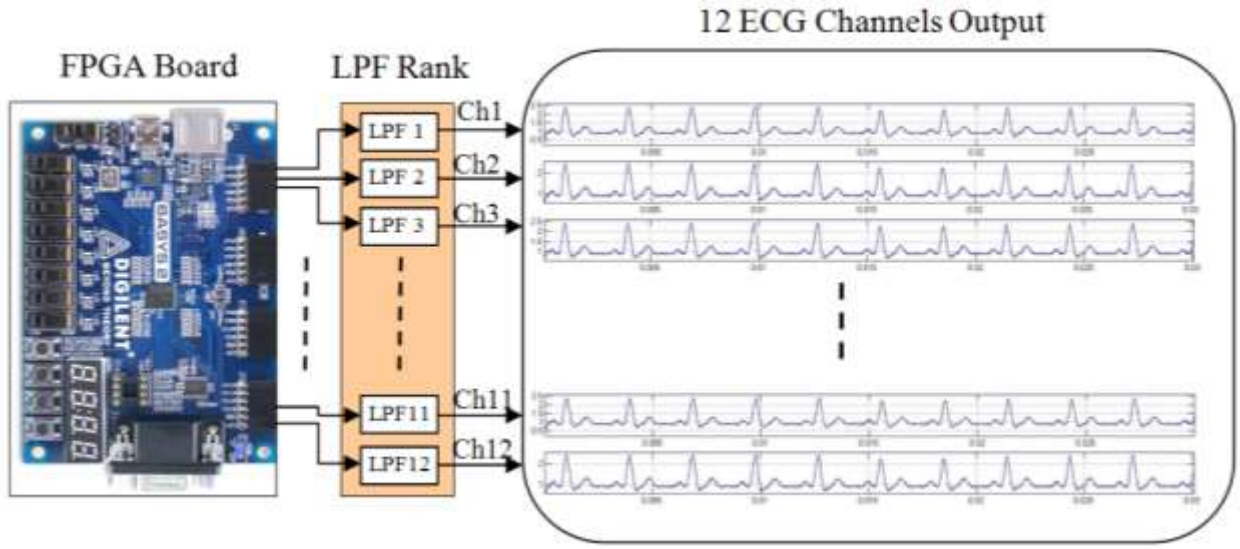

Figure 11: The complete system diagram

Table 1 shows the FPGA utilisation summary for the completed system, this also shows that the hardware cost of the system is low.

Table 1: Xilinx Spartan 3E Utilisation Summary.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	54	960	5%
Number of Slice Flip Flops	36	1920	1%
Number of 4 input LUTs	79	1920	4%
Number of bonded IOBs	9	83	10%
Number of MULT18X18SIOs	2	4	50%
Number of GCLKs	1	24	4%

CONCLUSION

This work describes a system capable of flexible and accurate signal generation making use of the spreading effect seen in scrambled PWM systems. The artificial ECG system described here allows wide ranging tests to be carried out without the need for a real person and cost issues associated with real experimentation, moreover, the linearisation module of the PWM system provides a novel method to improve the frequency response of a smoothed PWM output that may be applicable in many other application spaces. The flexibility of the FPGA is the key to making this modification to the PWM component possible.

In addition, this system is capable to produce multi-ECG with heart rate from 60 - 90 bpm range for wide range of testing. Moreover, the ECG waveform can be easily controlled with using USB interface controller.

Further, it worth to mention that, the algorithm improvements does not cost the FPGA board large number of logic gates. As well as, using one bit PWM instead of multiple bits offer extra saving in I/O ports and hardware required for the design within the FPGA.

REFERENCES

[1] De Luca, C.J., "Physiology and Mathematics of Myoelectric Signals," in Biomedical Engineering, IEEE Transactions on , vol.BME-26, no.6, pp.313-325, June 1979.
[2] Patrick, S.; Meklenburg, J.; Jung, S.; Mendelson, Y.; Clancy, E.A., "An electromyogram simulator for myoelectric prosthesis testing," in Bioengineering Conference, Proceedings of the 2010 IEEE 36th Annual Northeast , vol., no., pp.1-,26-28 March 2010.
[3] A.I. Al-Shueli, C.T. Clarke, and J.T. Taylor, "Simulated Nerve Signal Generation for Multi-electrode Cuff System Testing," Biomedical Engineering and Biotechnology (iCBEB), 2012 International Conference on , vol., no., pp.892,896, 28-30 May 2012.
[4] A.I. Al-Shueli, C.T. Clarke, N. Donaldson, and J.T. Taylor, "Improved Signal Processing Methods for Velocity Selective Neural Recording Using Multi-Electrode Cuffs," Biomedical Circuits and Systems, IEEE Transactions on , vol.8, no.3, pp.401,410, June 2014.
[5] A.I. Al-Shueli, "Signal Processing for Advanced Neural Recording Systems," PhD Thesis, University of Bath, Bath, UK, 2013.
[6] Kiran Kumar Jembula et al, "Design Of Electrocardiogram (ECG Or EKG) System On FPGA", International Journal Of Engineering And Science ,Vol.3, No.2, pp 21-27, May 2013.
[7] K. a. Shehata, M. a. Aboul-Dahab, S. H. El Ramly, and K. a. Hamouda, "An FPGA based 1-bit all digital transmitter employing Delta-Sigma Modulation with RF output for SDR," 2008 2nd International Conference on Signals, Circuits and Systems, pp. 1–6, Nov. 2008.
[8] S. Hongzhi, W. Jie, M. Yichao, K. Yang, and Z. Jie, "A FPGA-based 7-order 1-bit Sigma-Delta Modulator for High-precision Signal Generation," in The Ninth International Conference on Electronic Measurement & Instruments, 2009, pp. 160–164.
[9] P. Kiss, J. Arias, D. Li, and V. Boccuzzi, "Stable High-Order Delta–Sigma Digital-to-Analog Converters," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 51, no. 1, pp. 200–205, Jan. 2004.
[10] Electrocardiography. In Wikipedia. Retrieved November 10, 2015, from https://en.wikipedia.org/wiki/Electrocardiography.